
Hardware mapping & data format study

- Learning basic things for
Data Formatter HW development -

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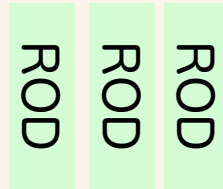
University of Chicago & Fermilab



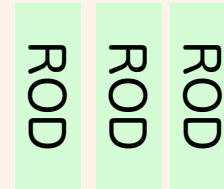
Data Formatter system

Challenging part
in the FTK application for ATLAS

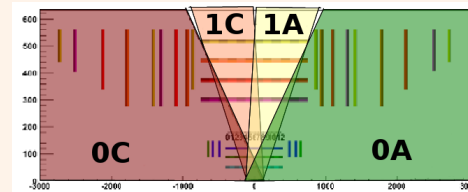
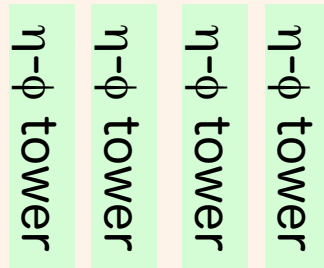
132 RODs Pixel



90 RODs SCT



Data Formatter
(222 RODs vs 64 towers)
Processed by 64 FPGAs mounted on 32 Boards



$$4 (\eta) \times 16 (\phi) = 64 \text{ towers}$$

Today's talk

I would like to show what I am learning:

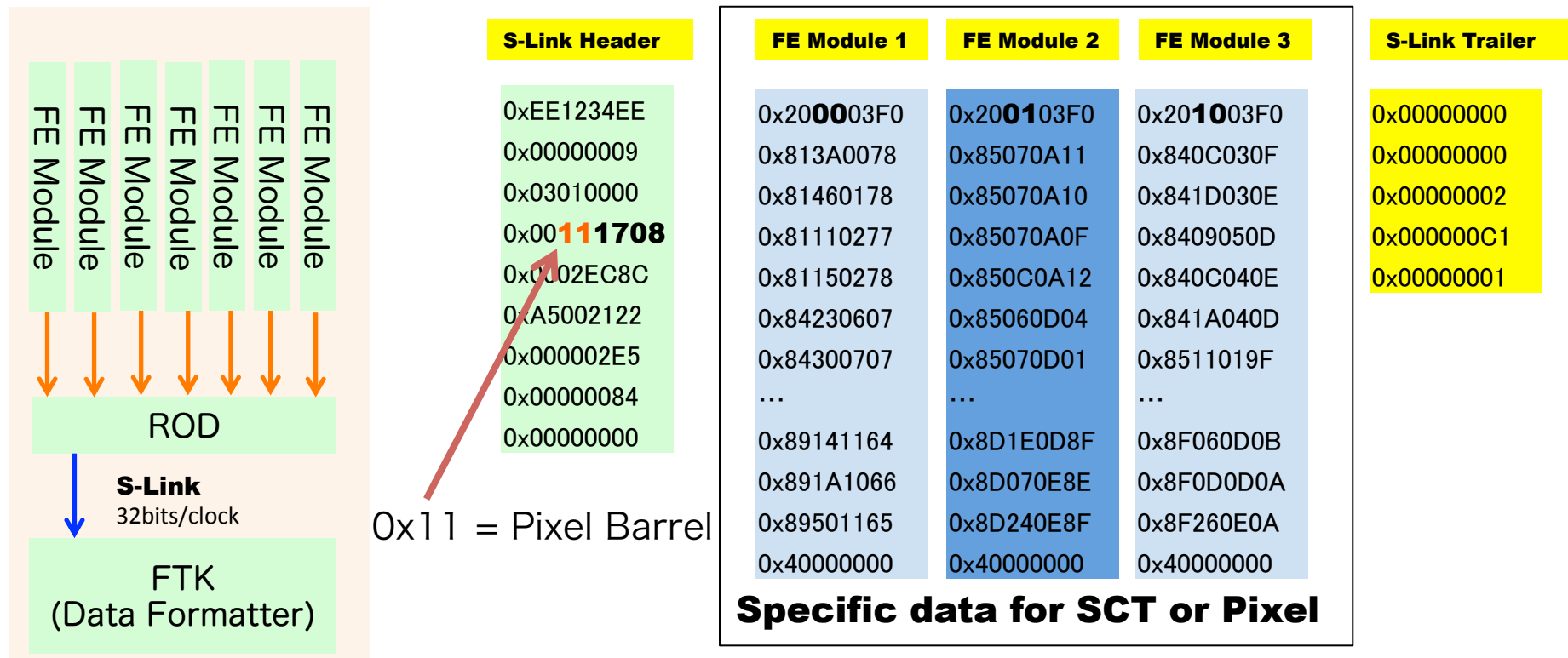
1. Study for data format from ROD (S-Link)
2. Study for detector – readout mapping from FTK application point of views
3. Initial look at data volume with beam collision data

Important basic knowledge for design, development, test, and commissioning

Data structure in S-Link

Series of 32 bits words from each of SCT/Pixel RODs

S-Link data structure



Data format of Pixel

Pixel raw data format detail

0x200003F0	0010 0000 0000 0000 0000 0011 1111 0000	→ Header Word
0x813A0078	1000 0001 0011 1010 0000 0000 0111 1000	→ Hit @ (0x00, 0x78)
0x81460178	1000 0001 0100 0110 0000 0001 0111 1000	→ Hit @ (0x01, 0x78)
0x81110277	1000 0001 0001 0001 0000 0010 0111 0111	→ Hit @ (0x10, 0x77)
0x81150278	...	
0x84230607	...	
0x84300707	...	
...	...	
0x89141164	...	
0x891A1066	...	
0x89501165	1000 1001 0101 0000 0001 0001 0110 0101	→ Hit
0x40000000	0100 0000 0000 0000 0000 0000 0000 0000	→ Trailer Word

Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	001			Errors				Module						Skipped L1ID				Level1 ID				BC ID										
Triler	010			Z	H	V	Bit Flip																									
Hit	100			BF	FE Number			Time over threshold value						Bit Flip				Column				Row										
Error	000			1	FE Number			-		1	1	1	1	1	MCC Error Code				FE Error Code													
Raw data	011			28 bits Raw Data																												
Timeout	001			0																												

Data format of SCT

SCT raw data format details

0x2001CAB3	0010 0000 0000 0001 → Header word 1100 1010 1011 0011 → Hit @ 0x2B
0xD41280BB	1101 0100 0001 0010 → Hit @ 0x41 1000 0000 1011 1011 → Neighboring 2 hits
0x80BB80BB	1000 0000 1011 1011 → Neighboring 2 hits 1000 0000 1011 1011 → Neighboring 2 hits
0x800BDD53	1000 0000 0000 1011 → Neighboring 1 hits 1101 1101 0101 0011
0xEE732002	1110 1110 0111 0011 0010 0000 0000 0010 → Header word

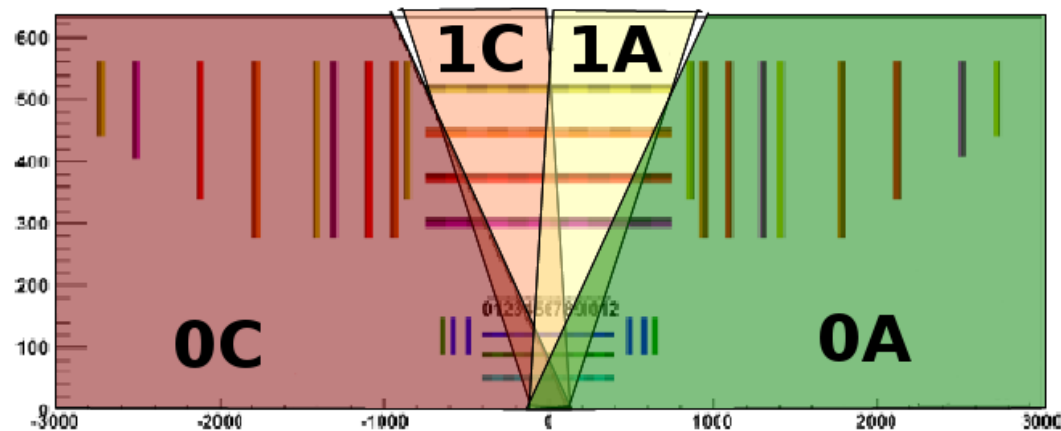
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	001			P	Level1 ID				Module							
Triler	010			Z	H	V	-									
1st Hit	1	sid	Chip ID		Cluster Base Address						0	Hit BC				
Neighbering hit (1)	1	-				0		-		1	Hit BC (1)					
Neighbering hit (2)	1	-				1		Hit BC (2)		1	Hit BC (1)					
Error	011			-						FE Number			Error Code			
Raw Data	001			#bits			-		Raw Data							

Hardware mapping

Mapping between Detector & Readout

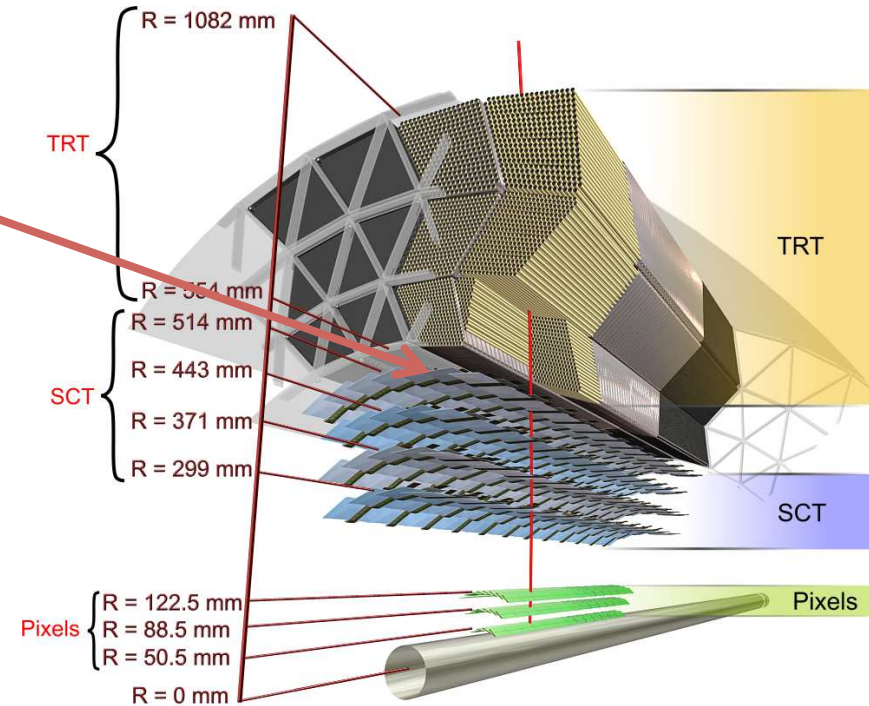
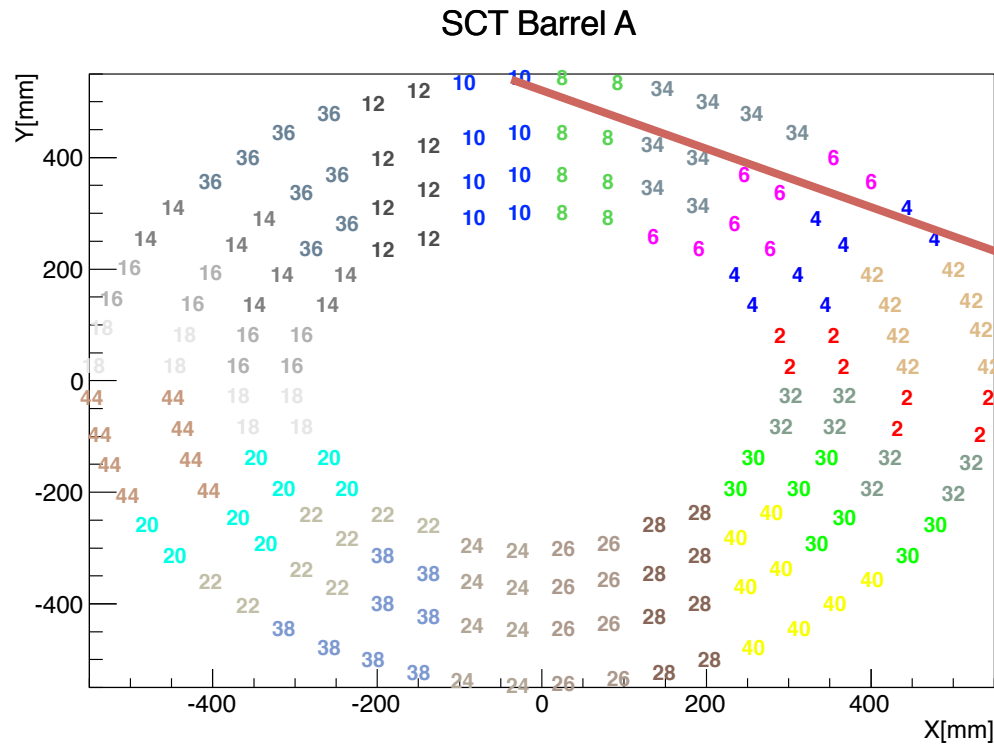
- Detector (x, y, z) - (Module & ROD) - FTK tower

Cabling of ID is complicating
Need to be understood for Data Formatter



Hardware mapping

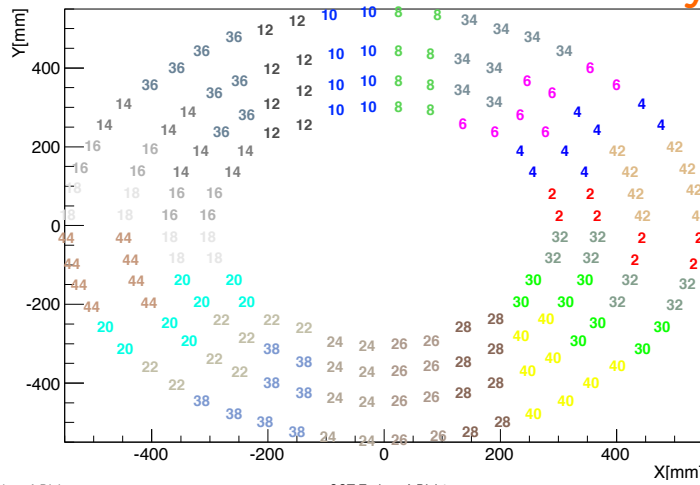
SCT Barrel ROD ID map



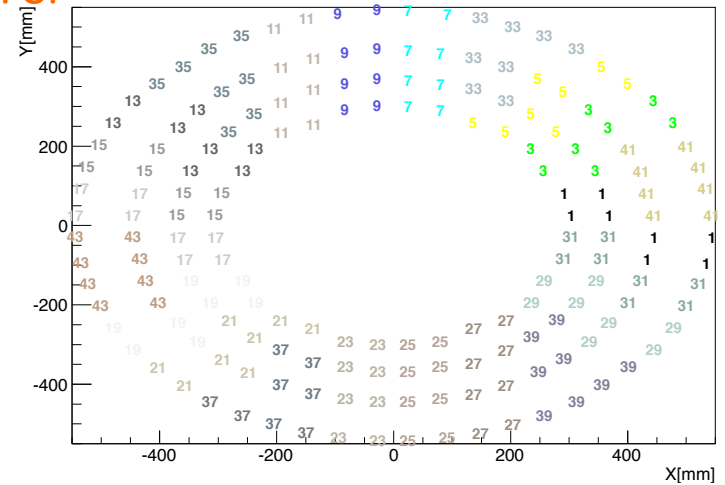
SCT (8176 Modules, 90 RODs)

SCT Barrel A

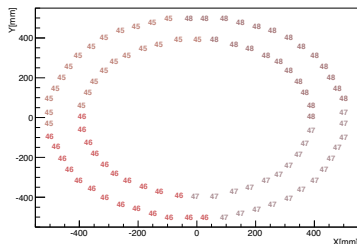
4 Layers in Barrel



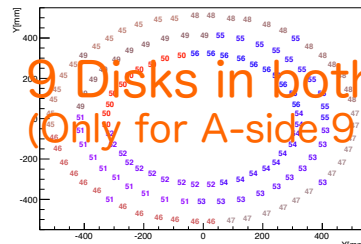
SCT Barrel C



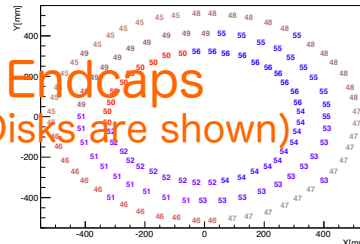
SCT Endcap A Disk1



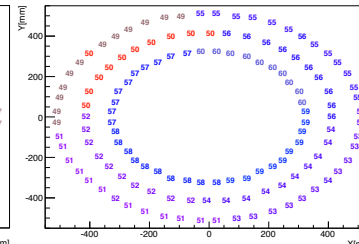
SCT Endcap A Disk2



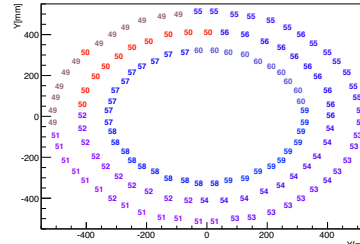
SCT Endcap A Disk3



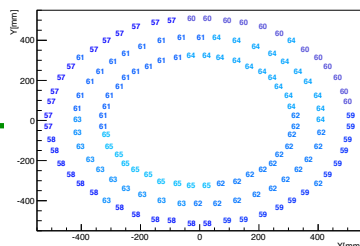
SCT Endcap A Disk4



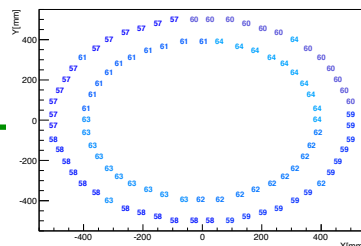
SCT Endcap A Disk5



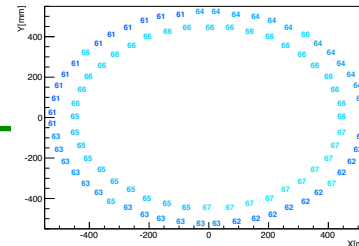
SCT Endcap A Disk6



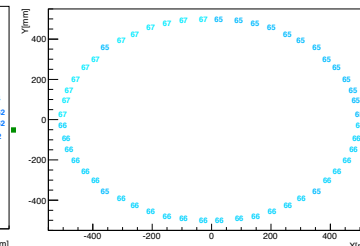
SCT Endcap A Disk7



SCT Endcap A Disk8



SCT Endcap A Disk9

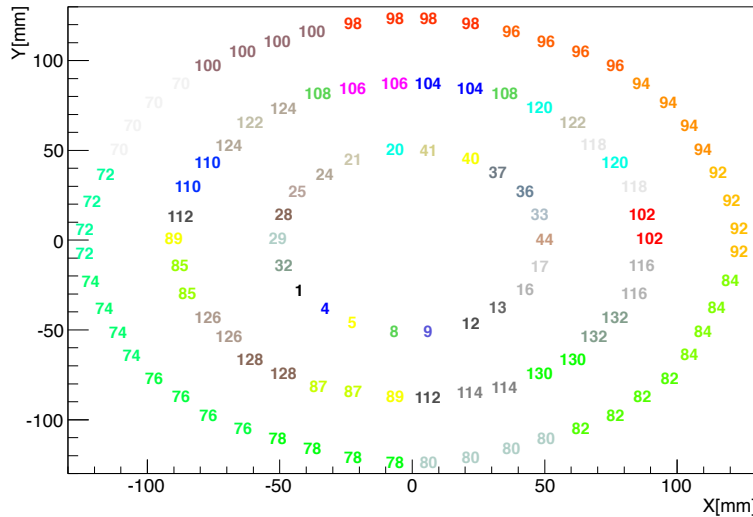


Hardware mapping

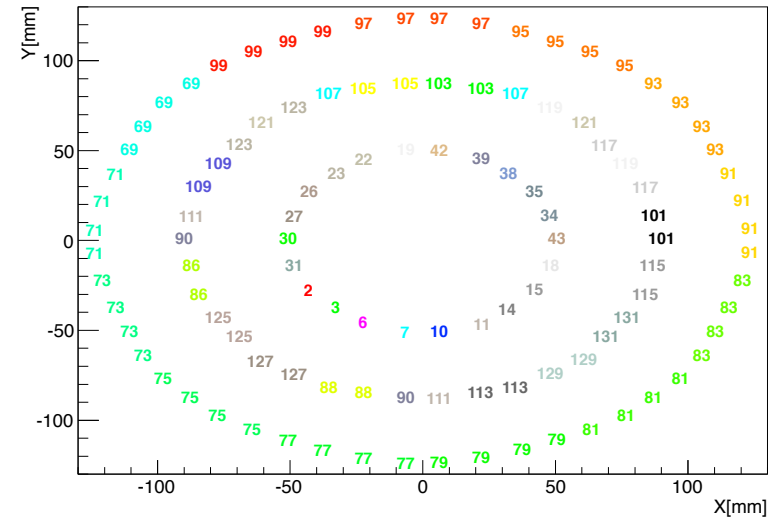
Pixel (1744 Modules, 132 RODs)

Pixel Barrel A

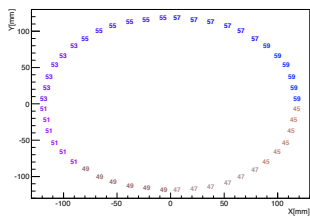
3 Layers in Barrel



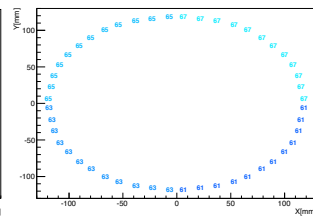
Pixel Barrel C



Pixel Endcap A Disk1

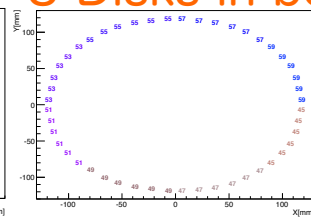


Pixel Endcap A Disk2

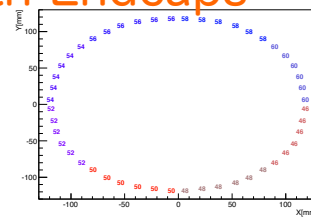


3 Disks in both Endcaps

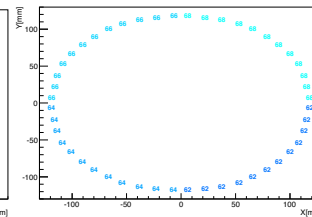
Pixel Endcap A Disk3



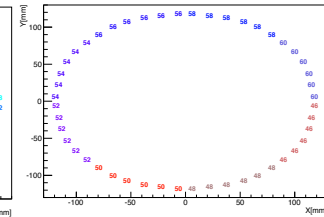
Pixel Endcap C Disk1



Pixel Endcap C Disk2

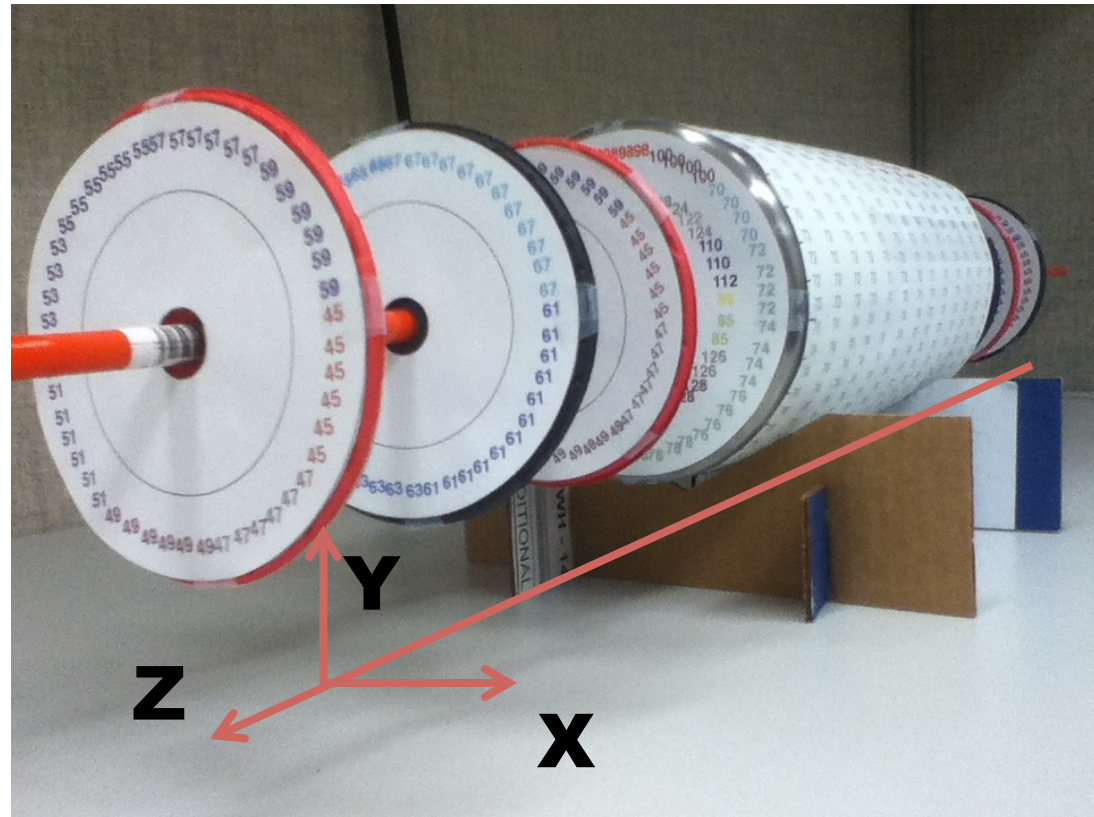
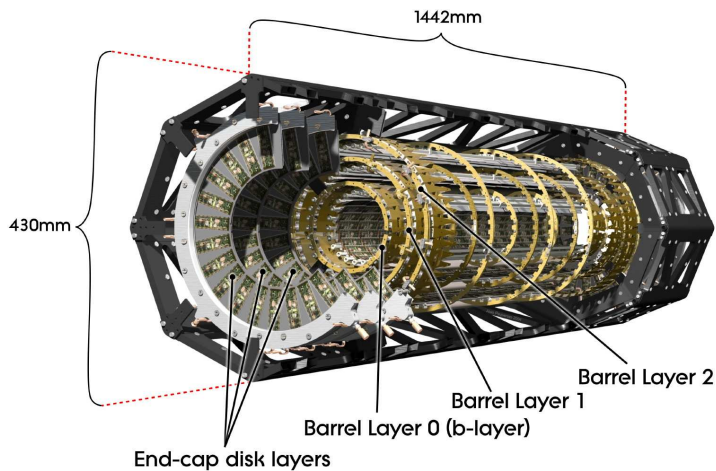


Pixel Endcap C Disk3



3D Pixel model

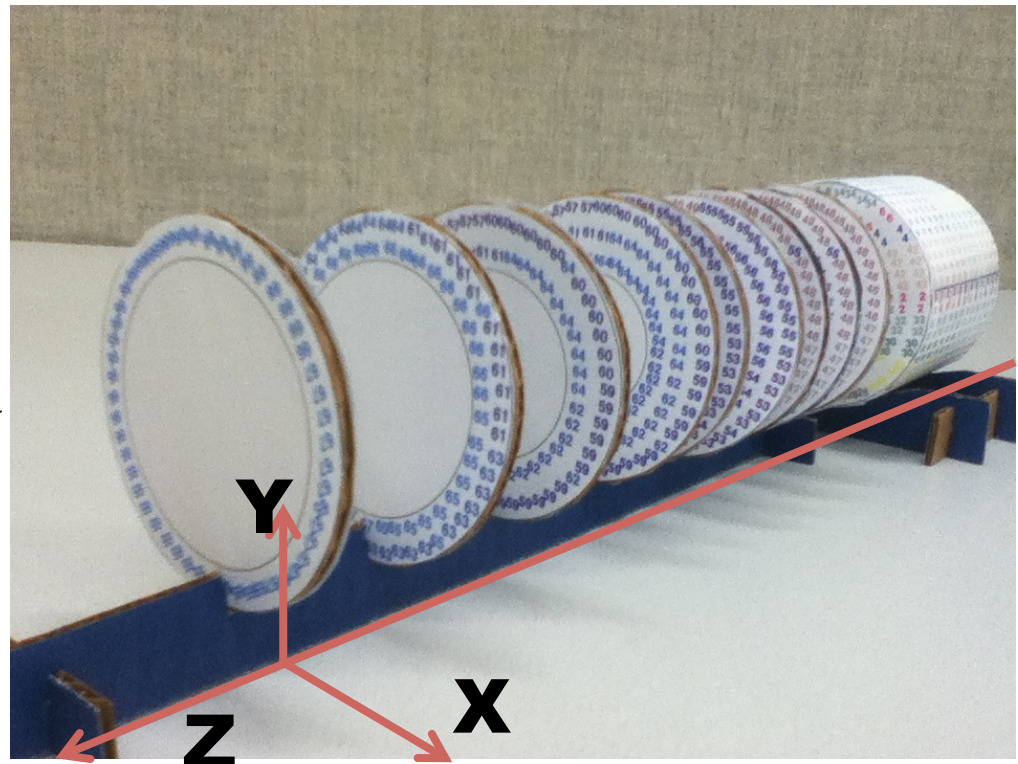
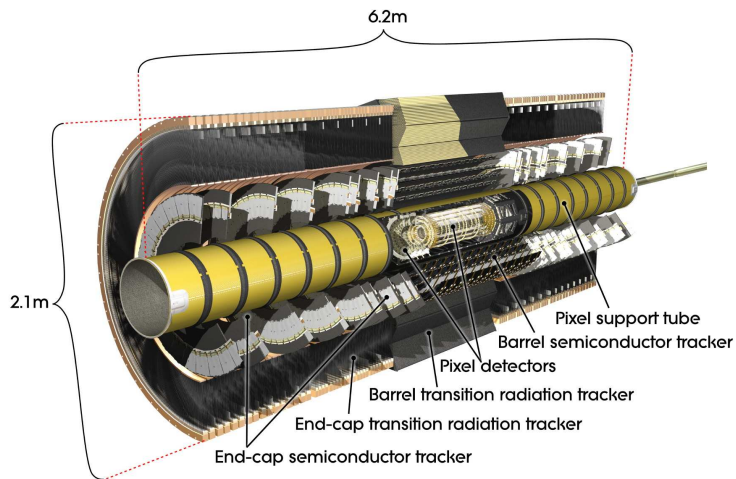
3D Pixel model with ROD ID mapping
(@Fermilab W/H 10)
(3 layers in Barrel, 3 disks in Endcap)



3D SCT model

3D SCT model ROD ID mapping (@Fermilab W/H 10)

(4 layers in Barrel, 9 disks in Endcap)



Initial look at real data

Next, we can look at
hits from each module with real data.

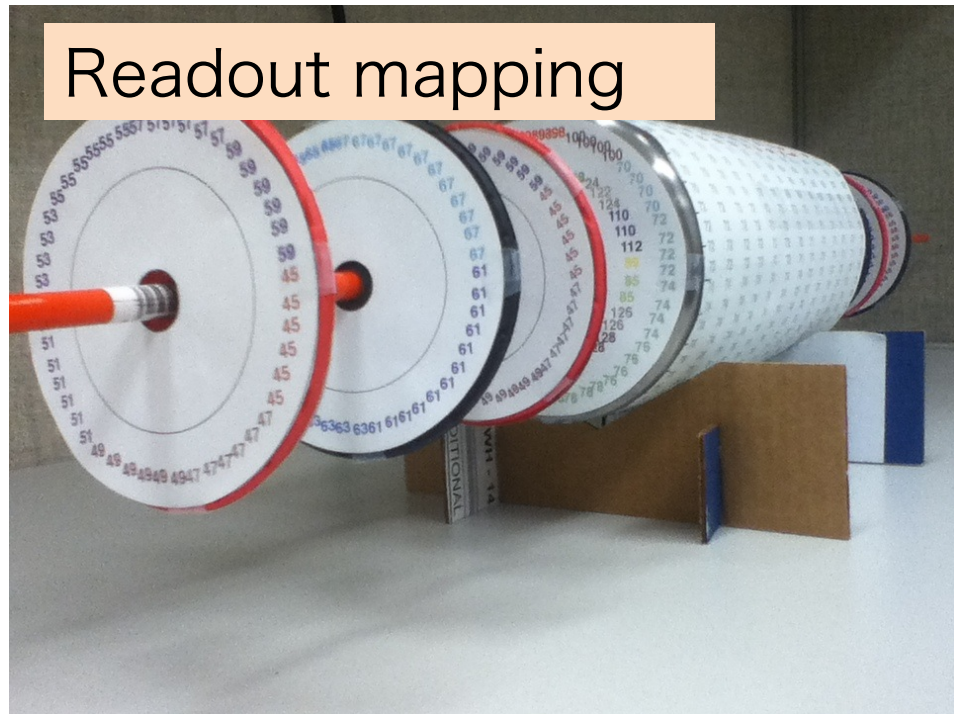
My private decoder on SVN:

https://svnweb.cern.ch/trac/atlasusr/browser/okumura/ftk/myPackage/bytestream_decoder/trunk

Raw data

```
0x200003F0  
0x813A0078  
0x81460178  
0x81110277  
0x81150278  
...  
0x89141164  
0x891A1066  
0x89501165  
0x40000000
```

Readout mapping



Data sample

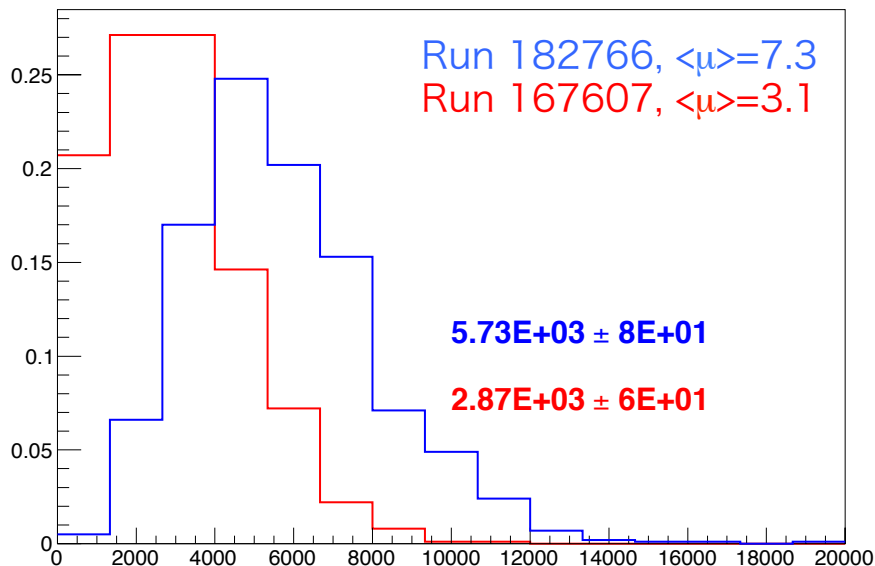
- Run 182766, Lumi-Block 225 (2011)
 - trigger : Egamma stream
 - Instantaneous luminosity : $1.0E33$
 - Number of bunches : 874 collisions @ P1
 - Pileup : $\langle\mu\rangle = 7.3$
 - Run 167607, Lumi-Block 159 (2010)
 - trigger : Egamma stream
 - Instantaneous luminosity : $1.7E32$
 - Number of bunches : 348 collisions @ P1
 - Pileup : $\langle\mu\rangle = 3.1$
-

#Hits/Event

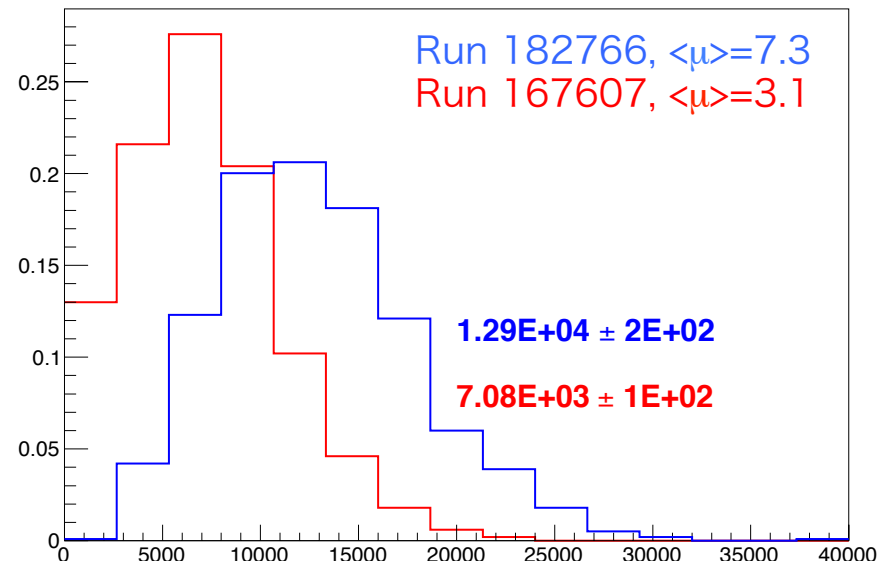
Pixel / SCT Hit multiplicity distributions

- Note : Numbers before clustering

Pixel Hit Multiplicity



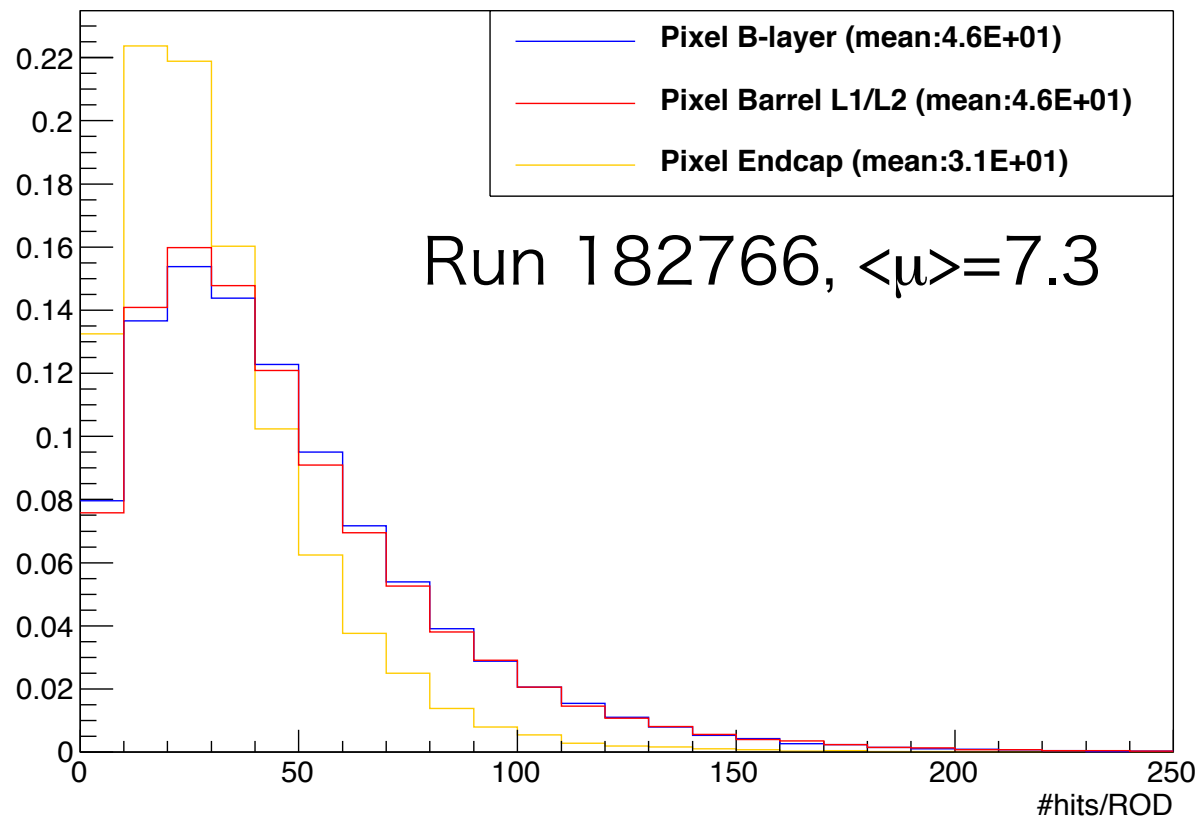
SCT Hit Multiplicity



#Hits/Event/ROD

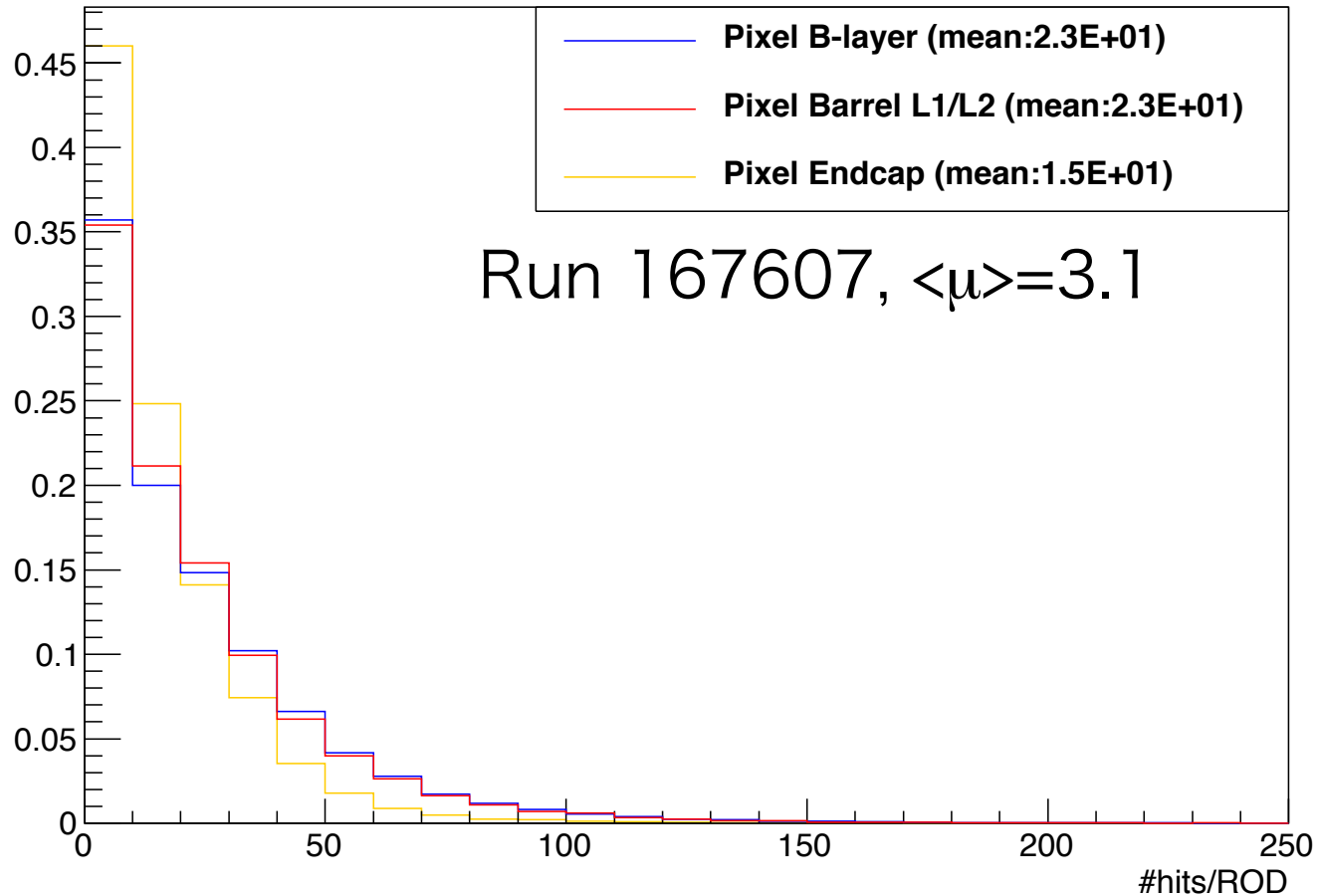
Number of Pixel hits per ROD per event

Note : Numbers before clustering



#Hits/Event/ROD

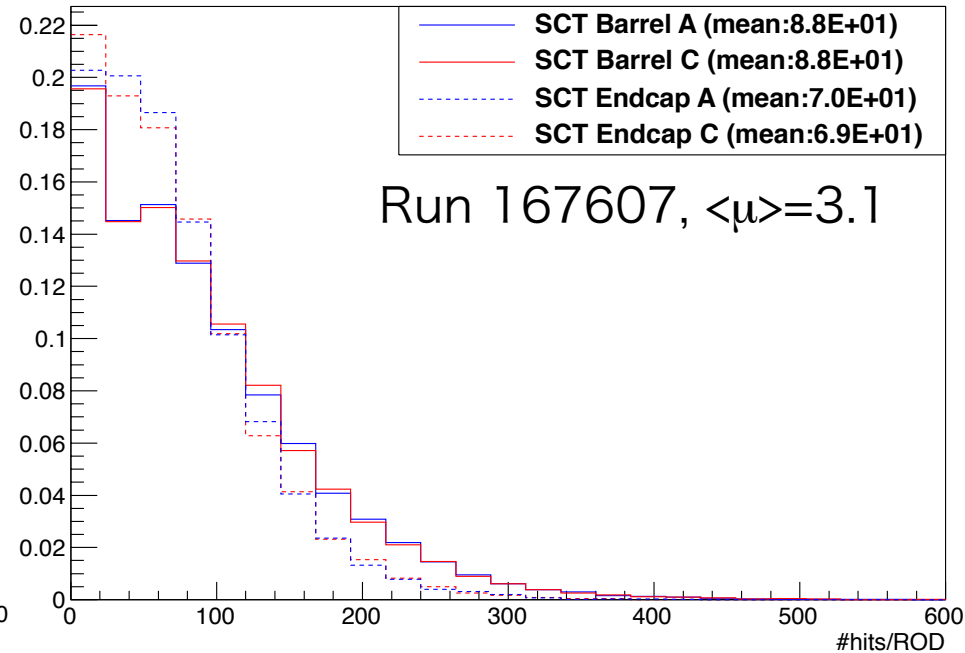
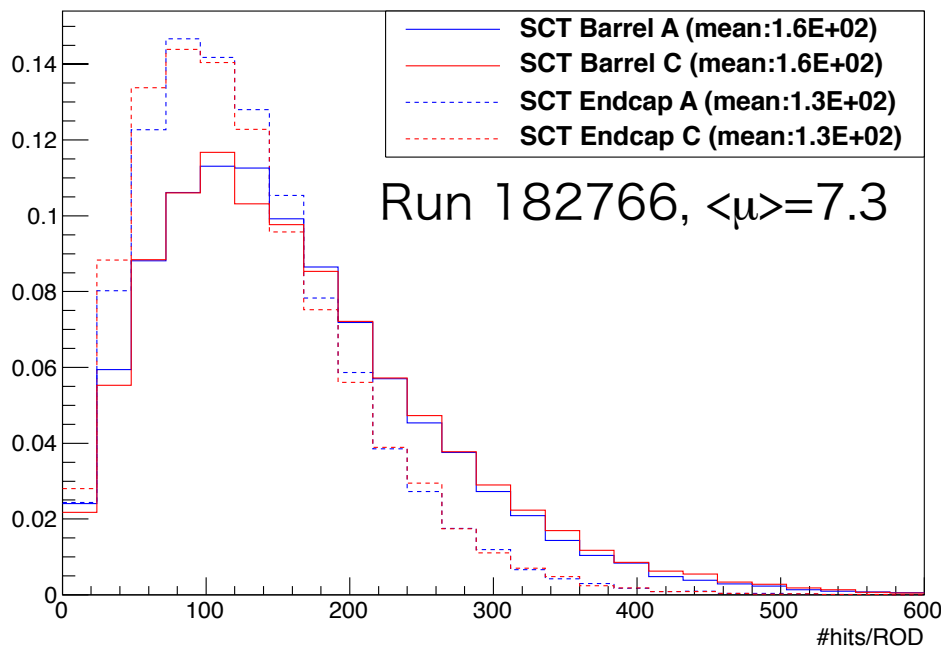
Same plot for low luminosity run



#Hits/Event/ROD

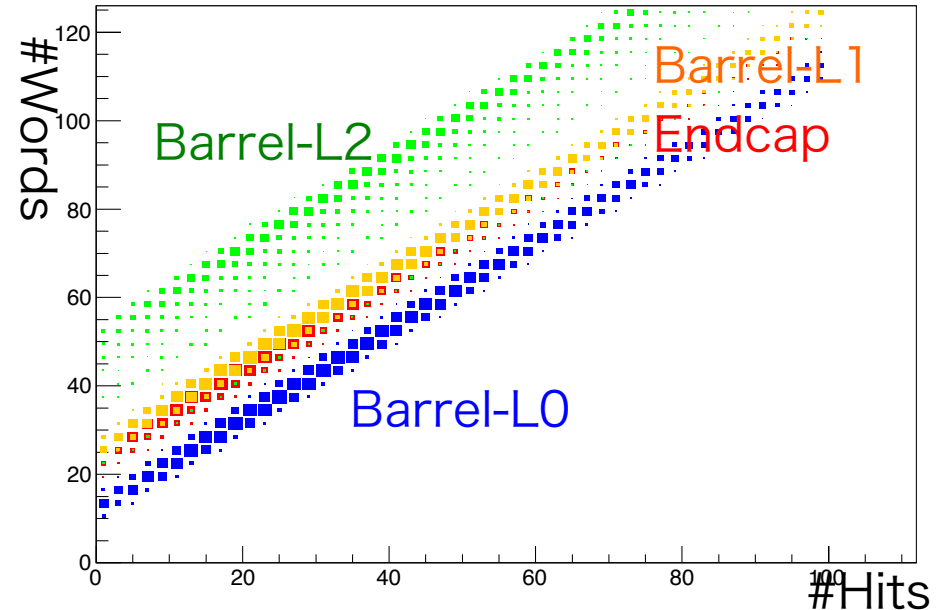
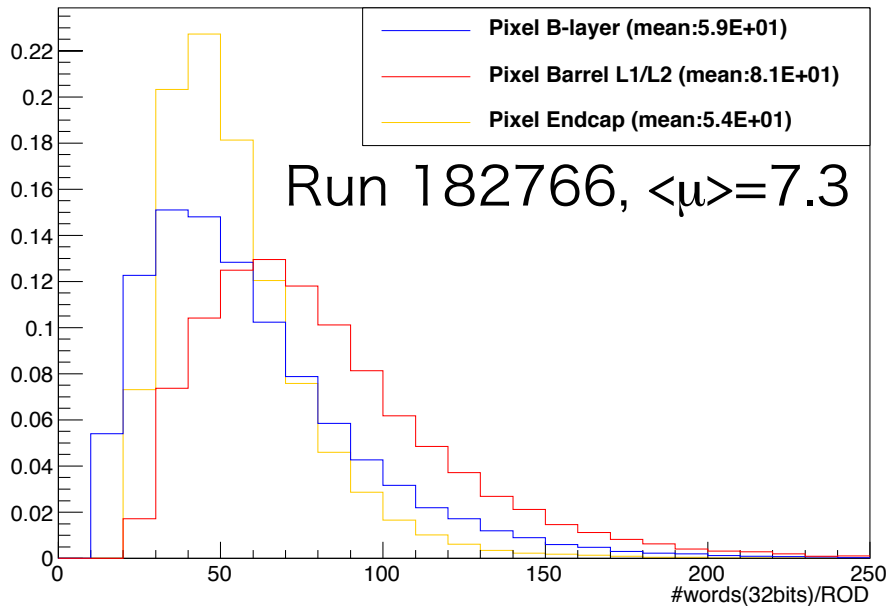
SCT Number of hits per ROD per Event

Note : Numbers before clustering



#Words/Event/ROD

Note: 1 Word is defined with 32 bits

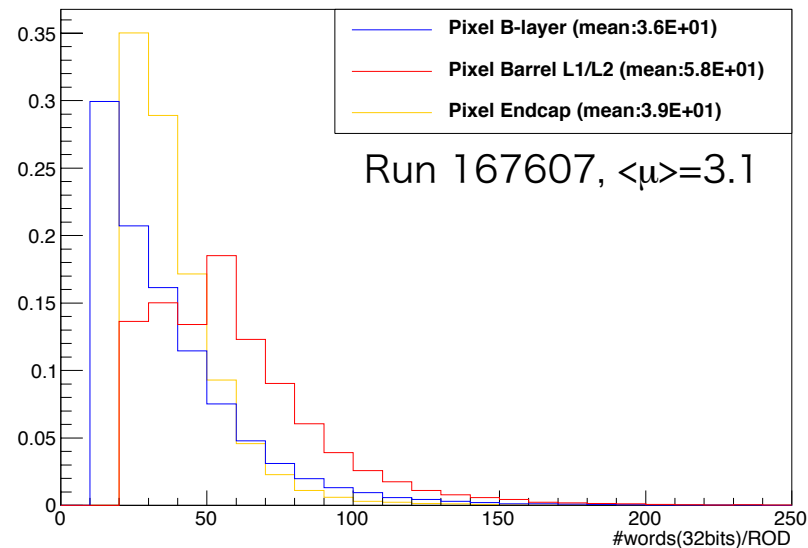
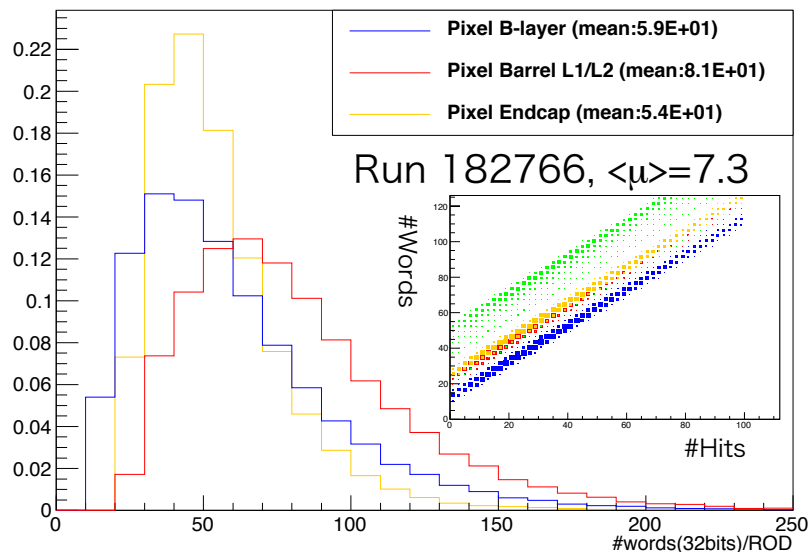


Number of modules per ROD

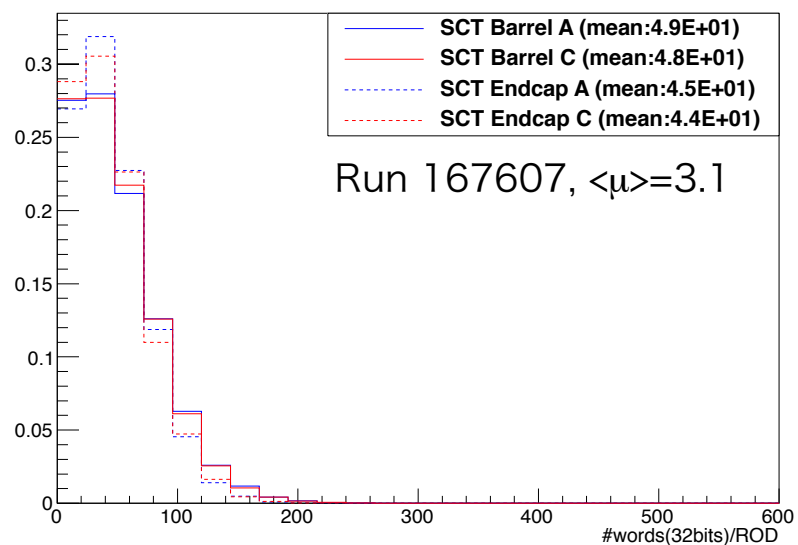
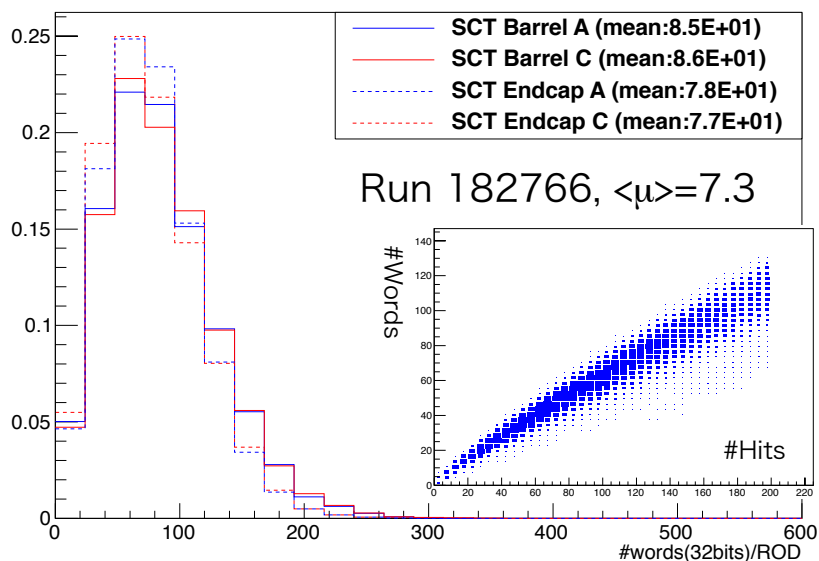
- Barrel L0 : 6-7 modules / ROD
- Barrel L1 : 13 modules / ROD
- Barrel L2 : 26 modules / ROD
- Endcap : 12 modules / ROD

#Words/Event/ROD

Pixel



SCT



Summary

Data formatter system is challenging

Started to learn about basics for the FTK system:

- Data format of S-Link
- Hardware mapping
- Initial look at real data

Much more will come in near future

Pixel coverage

Pixel Barrel Layout

#ROD = 22(A-L0), 19(A-L1), 13(A-L2)
 22(C-L0), 19(C-L1), 13(C-L2)

#ROD = 8(A-D1/D3), 4(A-D2), 8(C-D1/D3), 4(C-D2)

